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10/791,022	03/02/2004	Ta-Lee Yu	TS2000068BE	1284

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,022	YU, TA-LEE	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,33,35,37,38 and 47-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,33,35,37,38 and 47-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/16/2005 forms the basis for this office action. In said Amendment applicant amended the specification, cancelled claims 34 and 36, substantially amended all remaining previously outstanding claims 32-33, 35, 37-38, and added new claims 47-55.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "one of said second regions of said second conductivity dopant type is disposed between said alternating array and a top one of said first regions, and another of said second regions is disposed between said alternating array and a bottom one of said first regions" (final three lines of claim 32) must be shown or the feature canceled from claims 32-33, 35, 37-38 and 47-48.

Similarly, the limitation one of said second regions of said second conductivity dopant type is disposed between the alternating array and a top one of the first regions and another of the second regions is disposed between the alternating array and a bottom one of the first regions" (final three lines of claim 49) must be shown or the feature canceled from claims 49-55. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

   The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. ***Claims 32-33, 35, 37-38 and 47-48*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim contains subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The limitation "one of said second regions of said second conductivity dopant type is disposed between said alternating array and a top one of said first regions and another of said second regions is disposed between said alternating array and a bottom one of said first regions" is not disclosed in the original specification including claims and thus constitutes new matter. In particular, the second semiconductor layer 14 *overlying* said first conductivity layer 12 (line 6 of claim 32) implies the direction between top and bottom to correspond to the vertical direction in Figure 2 while only two parallel first regions 16 are disclosed at the same vertical position.

3. ***Claims 49-55*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim contains subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The limitation "one of said second regions of said second conductivity dopant type is disposed between the alternating array and a top one of the first regions and another of the second regions is disposed between the alternating array and a bottom one of the first regions" is not disclosed in the original specification including claims. In particular, the second semiconductor layer 14 overlying said first conductivity layer 12 (line 4 of claim 49) implies the direction between top

and bottom to correspond to the vertical direction in Figure 2 while only two parallel first regions 16 are disclosed at the same vertical position.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. ***Claims 32-33, 35, 37-38 and 47-48*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   In particular, the adjective "alternating" in "alternating array" (line 20 of claim 32) does not pertain to any feature of an array as such but instead requires specification of at least two different arrays to which alternating can be defined.

6. ***Claims 32-33, 35, 37-38 and 47-48*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   Said number "N" of said regions is claimed to "correspond" (claim 32, lines 21-22) to the number of multiple bipolar transistors, but the nature of the correspondence is left completely undefined, thus leading to indefinite claim language. A correspondence between one number and another can be made through any mapping in the space of numbers, in this case the set of natural numbers, without any lack of arbitrariness, yet a definite correspondence is recited by "corresponds", which makes the claim language indefinite.

7. ***Claims 49-55*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Said number "N" of said regions is claimed to "correspond" (claim 32, lines 21-22) to the number of multiple bipolar transistors, but the nature of the correspondence is left completely undefined, thus leading to indefinite claim language.

8. ***Claims 49-55*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In particular, the adjective "alternating" in "alternating array" (claim 49, line 16) does not pertain to any feature of an array as such but instead requires specification of at least two different arrays to which alternating can be defined.

9. Regarding ***claim 36***, the phrase "like" in "box like" (line 3) renders the claim indefinite because the claim includes elements not actually disclosed (those encompassed by "like"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).
10. Regarding ***claim 52***, the phrase "like" on "box like" (line 3) renders the claim indefinite because the claim includes elements not actually disclosed (those encompassed by "like"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. ***Claims 32-33, 37-38, 47, 49-50 and 52-54*** are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al.

The following rejections are provided subject to the noted indefiniteness as explained above under 35 U.S.C. 112, second paragraph, and are based on the best understanding of examiner given the circumstances.

Chen et al teach (Figure 4, title, abstract, and cols. 1-5) an integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate 42 (col. 3, l. 35-36) (title and abstract; Figure 4 and cols. 2-4), functionally connected between an integrated circuit input or output pin 34 (col. 3, l. 5) and ground (indicated in Figure 4) which will prevent electrostatic discharge damage to said integrated circuit comprising;

a first semiconductor layer 44 (col. 3, l. 35) having a first conductivity dopant type (N-type);

a second semiconductor layer (central Nwell portion of 46) (col. 3, l. 40-42) overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant concentration (N instead of N+);

a third semiconductor layer 62 (col. 3, l. 62) having a second conductivity dopant type opposite that of said first semiconductor layer (P-type), disposed in overlying relation to said second semiconductor layer (cf. Fig. 4);

a plurality of first regions (50 and abutting remnant of 46 separated from Nwell 46 to the outside of 50; see Figure 4) (col. 3, l. 47-50) of said first conductivity type (N-type) electrically connecting with said first semiconductor layer, having a top element 58 (col. 3, l. 59) making electrical contact to said first regions and said first semiconductor layer (col. 3, l. 55-59);

a plurality of second regions 64 and 56 (col. 3, l. 53-60 and 63) of said second conductivity dopant type (P-type) laterally spaced from said first regions (cf. Fig. 4), being electrically connected to said third semiconductor layer having a top element 76 making electrical contact to said second regions and said second semiconductor layer (see Figure 4);

a plurality of third regions 66 (col. 4, l. 4) of said first semiconductor layer conductivity dopant type (N-type) laterally spaced and interposed between said second regions,

wherein one of said second regions 64/56 of said second conductivity dopant type (namely: element 56 either to the right or left of center in Figure 4) is disposed between said alternating array and a top one of said first regions (namely: the element 50 itself, either to the right or the 50 to the left of center in Figures 4 and 6, respectively), and another of said second regions (namely: said element 56 to the left or the right of center in Figure 4) is disposed between said alternating array and a bottom one of said first regions (namely: said remnant of

62 separated from 62 to the outside by 50, to the left or right of center in Figure 4, respectively).

The limitation "that comprise said ESD protection structure" in claim 32 is (a) met by Chen because of the specific teaching (see e.g. also col. 1, l. 50-64) and (b) because of the inherent property of any npn structure to protect against any voltage independent of its bias since one of the n-p interfaces is always reverse biased.

In conclusion, Chen et al anticipates claims 32 and 49.

On claims 33 and 50: the plurality of first regions 50 (+remnant of Nwell 46 as defined above) together with the associated connected first semiconductor layer 44 are with n dopant and form multiple collector elements of a bipolar transistor in which the bases are formed by said third semiconductor layer 62 and associated said plurality of second regions of p dopant, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions 66 of n type dopant (cf. Figures 4 and 6: N.B. 65 are the emitter contacts (col. 3, l. 64)).

On claims 37 and 52: the third regions 66 are electrically connected by a conductor element with horizontal stripe conductor elements, for each element of the array holding N elements (see definition as implicit in amended claim language of claims 32 and 49, respectively) in total, there is one aforementioned horizontal stripe conductor element (indented, lower plateau portion of polysilicon 68 (col. 4, l. 5) and connected in a contiguous manner (otherwise no voltage could be sustained and no current could flow) by contact conductor

elements with vertical extension (see Figure 4: elements 68, loc.cit.), hence qualifying as "vertical contact conductor elements", at both ends of said horizontal emitted conductor stripes.

On claims 38, 47, 53 and 54: the plurality of the (or, in the alternative: said) second regions 64 and 56 and said third regions 66 are ultimately connected together (see wire 60 from 66/65 through connected to 56 and connected through wire 76 to 64) (Figure 4) and to a second voltage source that is ground (claims 47 and 54 are thus also met).

On claims 48 and 55: the third regions 66 are electrically connected by a conductor element 68 (col. 4, l. 5) with N horizontal stripe conductor elements (each horizontal strip being indented portion of 68 positioned lower than a high-level plateau (see Figure 4)), and at least two of the horizontal stripe conductor elements are connected by at least one first vertical contact conductor element (contact between 68 and 66) (Figure 4) at one end of the horizontal stripe conductor elements (bottom end of the far left end of array 66 in Figure 4), and at least two of the horizontal stripe conductor elements are connected by at least one second vertical contact conductor element at another end of the horizontal stripe conductor elements (bottom end of the far right end of array 66 in Figure 4) so that the horizontal stripe conductor elements are connected to each other.

Double Patenting

12. ***Claims 49-51*** are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 32, 33, 35 respectively.

The claims are so close in content that they both cover the same thing, despite a slight difference in wording, because the omission of the limitation "that comprise said ESD protection structure" (lines 22-23 of claim 32) in claim 49 does not change the substance of the content of the claim, because a parallel transistor array of multiple bipolar transistors is an ESD protection structure, an npn structure always provides protection against ESD: one of the interfaces in the npn structure always being reverse biased given any voltage across it. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim.

See MPEP § 706.03(k).

Response to Arguments

Applicant's arguments filed 11/16/05 have been fully considered but they are not persuasive.

The amendments to the specification have been approved.

On Claim objections: said objections have been overcome by amendment.

On Claim Rejections under 35 U.S.C. 112, second paragraph: "alternating", according to the Oxford Dictionary has the following complete list of meanings: (a) succeeding each other by turns"; (b) occurring in alternation to something else; (c) consisting of alternations; and (d) reversing direction at regular intervals (see Oxford Dictionary). The latter meaning is excluded because of context while all meanings (a), (b) and (c) require two things, whether to

succeed in turns, occurring in alternation with something else, or consisting of alternations. Therefore, "alternating" within the context of the substantially amended language is again considered indefinite.

On claim 37, no such amendment has been found in the claim language, which still states: "box like". Hence a rejection based on said claim language is again included.

On Remarks on the rejection under 35 U.S.C. 102(b): applicant's argument is not based on a refutation of Chen et al.

New claims and substantially amended claims are presently examined for the first time.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 27, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER